IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): William G. America et al.

Examiner: Jack S. J. Chen

Serial No: 10/674,646

Art Unit: 2813

Filed: September 30, 2003

Docket: YOR920030320US1 (16868)

For: PLASMA SURFACE MODIFICATION AND PASSIVATION OF ORGANO-SILICATE GLASS FILMS FOR IMPROVED HARDMASK ADHESION AND OPTIMAL RIE PROCESSING

Confirmation No. 4797

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION PURSUANT TO 37 C.F.R. §1.131

Sir:

We, William G. America, Timothy J. Dalton, Kaushik A. Kumar and Heidi L. Baks, hereby declare that:

1. We are co-inventors of the subject matter described and claimed in the above-identified patent application.

2. Prior to May 27, 2003, which is the effective filing date of U.S. Patent No. 6,927,159 to Faust et al. ("Faust et al."), we have conceived and reduced to practice a semiconductor structure such as, an interconnect structure, that comprises one or more interconnect levels, one on top of each other, each level comprising an organo-silicate glass (OSG) dielectric material having a plasma treated surface layer that provides improved

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adhesion to an overlying lower hardmask, yet is substantially undamaged, as is recited in Claim 1 of the present application.

3. As evidence of the conception and reduction to practice of the claimed semiconductor structure referred to in paragraph 2 prior to the effective filing date of Faust et al., annexed hereto are Exhibits A and B. Exhibit A is a true reprint in PDF format of IBM Invention Disclosure YOR820030277, which was created prior to May 27, 2003. Exhibit A includes a Main Idea section for the Invention Disclosure which describes the fabrication of a semiconductor structure such as an interconnect structure that is recited in Claim 1 of the present application. Exhibit B is the inventors' write-up of the Disclosure that was also created prior to the effective filing date of Faust et al. This write-up provides greater detail of the invention presently claimed including experimental data that establishes clear evidence of actual fabrication of the claimed semiconductor structure. All names and dates have been redacted in the preparation of this Declaration.

4. We do hereby declare that all statements made herein of our own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that such willful false statements may jeopardize the validity or enforceability of the patent.

8 April 2006
Dated

William G. America

Dated

Timothy J. Dalton

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3. As evidence of the conception and reduction to practice of the claimed semiconductor structure referred to in paragraph 2 prior to the effective filing date of Faust et al., annexed hereto are Exhibits A and B. Exhibit A is a true reprint in PDF format of IBM Invention Disclosure YOR820030277, which was created prior to May 27, 2003. Exhibit A includes a Main Idea section for the Invention Disclosure which describes the fabrication of a semiconductor structure such as an interconnect structure that is recited in Claim 1 of the present application. Exhibit B is the inventors' write-up of the Disclosure that was also created prior to the effective filing date of Faust et al. This write-up provides greater detail of the invention presently claimed including experimental data that establishes clear evidence of actual fabrication of the claimed semiconductor structure. All names and dates have been redacted in the preparation of this Declaration.

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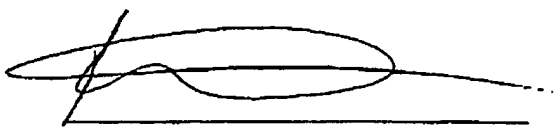
Dated

William G. America

7 Apr. 2006

Dated



Timothy J. Dalton

Apr 10, 2006
Dated

Kaushik A. Kumar

Dated

Kaushik A. Kumar

4/10/06
Dated

Heidi L. Baks

Applicant(s): William G. America et al.

Examiner: Jack S. J. Chen

Serial No: 10/674,646

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For: PLASMA SURFACE MODIFICATION AND PASSIVATION OF ORGANO-SILICATE GLASS FILMS FOR IMPROVED HARDMASK ADHESION AND OPTIMAL RIE PROCESSING

Confirmation No. 4797

Exhibit A

Disclosure YOR8-2003-0277

Prepared for and/or by an IBM Attorney - IBM Confidential

***Title of disclosure (in English)**

Plasma surface modification and passivation of porous organo-silicate glass (p-OSG) films for improved hardmask adhesion and optimal RIE processing

Summary

Status	Final Decision (File)
Docket Family	YOR9-2003-0320
*Processing Location	YOR
*Functional Area	(703B) 703B INTERCONNECT TECHNOLOGY
Attorney/Patent Professio1	
IDT T	
Submitted Date	
*Owning Division	RES
Lab	
*Technology Code	1011

Inventors with a Blue Pages entry

Inventors without a Blue Pages entry

IDT Selection

YOR8-2003-0277 Plasma surface modification and passivation of porous organo-silicate glass (p-OSG)

***Main Idea**

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.

***Critical Questions (Questions 1-9 must be answered in English)**

***Question 1**

On what date was the invention workable? **Please format the date as MM/DD/YYYY**
(Workable means i.e. when you know that your design will solve the problem)

***Question 2**

Is there any planned or actual publication or disclosure of your invention to anyone outside IBM? ○ Yes ● No

If yes, Enter the name of each publication or patent and the date published below.
Publication/Patent:
Date Published or Issued:

Are you aware of any publications, products or patents that relate to this invention? ○ Yes ● No

If yes, Enter the name of each publication or patent and the date published below.
Publication/Patent:
Date Published or Issued:

***Question 3**

Has the subject matter of the invention or a product incorporating the invention been sold, used internally in manufacturing, announced for sale, or included in a proposal? ○ Yes ● No

Is a sale, use in manufacturing, product announcement, or proposal planned? ○ Yes ● No

If Yes, identify the product if known and indicate the date or planned date of sale, announcements, or proposal and to whom the sale, announcement or proposal has been or will be made.
Product:
Version/Release:
Code Name:

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YOR8-2003-0277 Plasma surface modification and passivation of porous organo-silicate glass (p-OSG)

Date:
To Whom:
If more than one, use cut and paste and append as necessary in the field provided.

***Question 4** ○ Yes ● No
Was the subject matter of your invention or a product incorporating your invention used in public, e.g., outside IBM or in the presence of non-IBMers?
If yes, give a date. **Please format the date as MM/DD/YYYY**

***Question 5** ○ Yes ● No
Have you ever discussed your invention with others not employed at IBM?
If yes, identify individuals and date discussed. Fill in the text area with the following information, the names of the individuals, the employer, date discussed, under CDA, and CDA #.

***Question 6** ○ Yes ● No ○ Not sure
Was the invention, in any way, started or developed under a government contract or project?
If Yes, enter the contract number

***Question 7** ○ Yes ● No ○ Not Sure
Was the invention made in the course of any alliance, joint development or other contract activities?
If **Yes**, enter the following:

Name of Alliance, Contractor or Joint Developer	
Contract ID number	
Relationship contact name	
Relationship contact E-mail	
Relationship contact phone	

***Question 8** ○ Yes ● No
Have you, or any of the other inventors, submitted this same invention disclosure or similar invention disclosure previously?
If Yes, please provide disclosure number below:

***Question 9** ○ Yes ● No
Are you, or any of the other inventors, aware of any related inventions disclosures submitted by anyone in IBM previously?
If Yes, please provide the docket or disclosure number or any other identifying information below:

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Question 10
What type of companies do you expect to compete with inventions of this type? *Check all that apply.*

- ☐ Manufacturers of enterprise servers
- ☐ Manufacturers of entry servers
- ☐ Manufacturers of workstations
- ☐ Manufacturers of PC's
- ☐ Non-computer manufacturers
- ☐ Developers of operating systems
- ☐ Developers of networking software
- ☐ Developers of application software
- ☐ Integrated solution providers
- ☐ Service providers
- ☒ Other (Please specify below)

Microelectronics companies

Question 11
If the invention relates to a product or service that is outside the scope of your business unit, please recommend IBM business unit(s), IBM location(s) or individual(s) within IBM that you think would provide a good evaluation of your invention:

***Patent Value Tool (Optional - this may be used by the inventor and attorney to assist...**

(The Patent Value tool can be used by the inventor(s) to determine the potential licensing value of your invention.)

Market

***Question 1:** What is the anticipated annual market size (in dollars) that will be captured by your invention?
$10M to $100M
Reason(s) for above Answer:

Claims

***Question 1:** How new is the technical field?
Emerging
Reason(s) for above Answer:

***Question 2:** How central is the invention to the product(s) which might be expected to contain the invention?
Essential
Reason(s) for above Answer:

***Question 3:** What is the scope of the claim?
Moderate
Reason(s) for above Answer:

Portfolio Need

***Question 1:** What are the portfolio needs in the area of your invention?
Listed in PPM Needs
Reason(s) for above Answer:

Exploitation & Enforcement

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YOR8-2003-0277 Plasma surface modification and passivation of porous organo-silicate glass (p-OSG)

Post Disclosure Text & Drawings

To add additional information related to this disclosure once it has been submitted, click the action button below and a new document will be opened for you to enter the new information. To view existing post disclosure information, double-click on the item in the list below (if there has been additional information entered), and the document will open for you to view.

Date entered	Post disclosure comments and drawings (double-click an item below to view)

(Form Revised 12/17/97)

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***Question 1:** How easily can the use of the invention by a competitor be detected?
With work
Reason(s) for above Answer:

***Question 2:** How easily can the use of the invention be avoided by a competitor?
With work
Reason(s) for above Answer:

Business Value
***Question 1:** What percentage of the companies producing products in the field of this invention might use this invention?
By 10% to 30%
Reason(s) for above Answer:

***Question 2:** What is the value of this patent to current or anticipated Alliance Activity between IBM and other companies?
High value
Reason(s) for above Answer:

***Question 3:** What is the value of this patent to current or anticipated Technology Transfer Activity between IBM and other companies?
High value
Reason(s) for above Answer:

***Question 4:** Does it result in prestige to IBM?
External
Reason(s) for above Answer:

Evaluation

Final Evaluation History	Who made the final evaluation	Final evaluation date

Final Decision

This decision was entered by

Decision: File	Status: N/A
PPM Area: 100	Attorney Rating:
Actual Release Date:	
Date of Final Decision	

Additional filing information

Planned Filing date:

Filing comments:

Additional decision comments

Final Decison History

Main idea for disclosure - continued

Main Idea for Disclosure YOR8-2003-0277

Prepared for and/or by an IBM Attorney - IBM Confidential

Title of disclosure (in English)

Plasma surface modification and passivation of porous organo-silicate glass (p-OSG) films for improved hardmask adhesion and optimal RIE processing

Idea of disclosure

1. Describe your invention, stating the problem solved (if appropriate), and indicating the advantages of using the invention.

When depositing CVD RIE hardmasks onto organosilicate (OSG) and porous organosilicate (p-OSG) dielectrics, adhesion is a significant issue. Insufficient adhesion of the hardmask will lead to delamination in CMP. This method of fabricating hardmask stack on p-OSG films alleviates the issues posed by adhesion of hardmask stack to the p-OSG film by incorporating an in-situ plasma treatment of the p-OSG dielectric prior to CVD hardmask deposition.

Additionally, CVD hardmasks such as SiC usually need a plasma densification process to prevent moisture absorption when the film is exposed to atmosphere prior to the next processing step. This densification layer has been found to cause micromasking during RIE processing. This proposal describes the deposition of another in-situ hardmask layer (SiN) to eliminate the need for densification of the first hardmask layer, thereby avoiding moisture absorption and avoiding subsequent RIE micromasking problems.

The surface modification of the p-OSG film and the deposition of subsequent hardmask layers (SiC and SiN, or other appropriate films), proposed in this invention, is done in-situ in a single deposition chamber.

2. How does the invention solve the problem or achieve an advantage,(a description of "the invention", including figures inline as appropriate)?

Hardmask stack:

Typical p-OSG film is capped by a SiC film which serves as a CMP stop layer. Typically, the top surface of this SiC film is densified in order to minimize the uptake of moisture by SiC. In order to protect the SiC film film from the oxygen-plasma based photoresist-strip process, a thin capping layer of SiN is used.

Issues with the fabrication sequence:

1. Untreated p-OSG film surface results in poor adhesion with the SiC capping layer.
2. SiC film is typically modified by He plasma treatment, which leads to a densification of the SiC surface. Densification of the SiC surface leads to micromasking in the trough-open step of the dual-damascene RIE process.
3. The SiC film is capped by SiN layer to protect the SiC layer from photoresist rework. The rework process involves an oxygen-plasma, which also etches the SiC film layer.

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Main idea for disclosure - continued

Solution proposed:
The p-OSG film is subjected to a brief He or other appropriate gas, plasma which modifies the film surface. This modified film surface ensures good adhesion with the SiC film layer. In order to preserve the modified p-OSG film surface, SiC is deposited in-situ on the surface-modified p-OSG film. The deposition of the SiC film is followed by the deposition of SiN film, in-situ, in order to prevent moisture uptake by the SiC film. This method eliminates the necessity of the densification of the SiC film. An example is:

p-OSG film -> He plasma treatment -> in-situ deposition of SiC film -> in-situ deposition of SiN film

Thus, a hardmask fabrication scheme is proposed that ensures good adhesion with the p-OSG film and also provides a simplified solution to the micromasking profile obtained during the trough-etch.

Novel HM process for RIE.PF

3. If the same advantage or problem has been identified by others (inside/outside IBM), how have those others solved it and does your solution differ and why is it better?

Identification of the problem:
1. He plasma treatment is known and has been implemented in the SiLK/SiCOH dual-damascene build in order to promote wetting and adhesion of SiLK on methylsilicones including CORAL and other similar films.
2. Less densified SiC film has been capped by N-doped SiC film, in order to prevent micromasking during trough-open. This has been implemented in the SiLK/USG dual-Damascene build. Unfortunately, this leads to a more complicated hardmask stack and SiC densification is not completely eliminated.

Difference in our solution:
The deposition of the SiC film occurs in-situ on the p-OSG film, resulting in a clean interface. SiN is deposited in-situ on SiC, resulting in the elimination of the N-doped SiC film while maintaining the integrity of the hardmask stack towards RIE and CMP processes. RIE and CMP processes do not have to address the non-uniformity of composition during processing that would result in differences in the rate and or final thicknesses of the films involved.

4. If the invention is implemented in a product or prototype, include technical details, purpose, disclosure details to others and the date of that implementation.

NO

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For: PLASMA SURFACE MODIFICATION AND PASSIVATION OF ORGANO-SILICATE GLASS FILMS FOR IMPROVED HARDMASK ADHESION AND OPTIMAL RIE PROCESSING

Confirmation No. 4797

Exhibit B

YOR8-2003-0277

PLASMA SURFACE MODIFICATION AND PASSIVATION OF POROUS ORGANO-SILICATE GLASS (p-OSG) FILMS FOR IMPROVED HARDMASK ADHESION AND OPTIMAL RIE PROCESSING

BACKGROUND OF THE INVENTION

1. Technical Field

The present invention generally relates to integrated circuits (ICs), and more particularly to interconnect structures, including multilevel interconnect structures, in which the adhesion of hardmasks to the underlying films is significantly improved by employing novel plasma treatments. The present invention is also directed to a method of fabricating an interconnect structure using an hardmask stack that has significantly improved adhesion with the underlying films, while enabling gentler reactive ion etch (RIE) patterning conditions.

2 Description of Related Art

Generally, semiconductor devices include a plurality of circuits which form an integrated circuit including chips (e.g., chip back end of line, or "BEOL"), thin film packages and printed circuit boards. Integrated circuits can be useful for computers and electronic equipment and can contain millions of transistors and other circuit elements that are fabricated on a single silicon crystal substrate. For the device to be functional, a complex network of signal paths will normally be routed to connect the circuit elements distributed on the surface of the device.

Efficient routing of these signals across the device can become more difficult as the complexity and number of the integrated circuits is increased. Thus, the formation of multi-level or multi-layered interconnection schemes such as, for example, dual Damascene wiring structures, have become more desirable due to their efficacy in providing high speed signal routing patterns between large numbers of transistors on a complex semiconductor chip. Within the interconnected structure, metal vias run perpendicular to the silicon substrate and metal lines run parallel to the silicon substrate.

Broadly, there are two limiting factors that affect the speed of signal propagation in the BEOL interconnects, namely, the resistance (R) of the wire and the capacitance (C) of the insulation between (also referred to as inter-layer-dielectric) the current carrying metal wires. The combination of these two factors manifests itself as interconnect or RC delay. One of the key challenges in the interconnect technologies is to reduce the electrical signal delay. This can be achieved by novel material changes, such as heading towards low dielectric constant (k) materials as the insulation material instead of the traditionally used silicon-dioxide films. Porous-Organo-Silicate Glass (pOSG) films, with k value lower than 3.0, are being investigated as a potential candidate material for thin wire integration.

In the integration of pOSG films, several dielectric films are deposited atop pOSG in order to serve as hardmasks, which are used in the fabrication of the trenches and vias. In order to fabricate a robust structure, the adhesion of the hardmasks with each other and to the pOSG films is critical. One common technique that is employed to enhance the adhesion between two films is a plasma-treatment of the underlying film prior to the deposition of the subsequent film. Typically, a plasma treatment roughens the underlying film at the microscopic dimensions, and hence increases the surface area for nucleation and or adhesion of the subsequent deposited film. However, in the case of pOSG films the open porosity on the surface of this film offers an

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increased surface area for the nucleation of the hardmask film. However, the adhesion is marginal and does not survive subsequent integration steps. Hence, a plasma treatment, by means of which a surface modification is achieved, is necessary to enhance the adhesion of the hardmasks to the pOSG film.

Another problem associated in the fabrication of robust structures using pOSG films lies in the identification of appropriate hardmask films. These hardmask films serve multiple purposes, such as, a chemical-mechanical polishing (CMP) stop layer, an oxygen diffusion barrier layer, etc. Typical films that are used as hardmask include silicon carbides (SiC) and related films of similar structure, such as hydrogenated-SiC and nitrogenated-SiC. These films serve as robust CMP-stop layers and also are good oxygen barriers. However, in order to maintain the oxygen barrier properties, the surface of the SiC film is densified after the deposition. This then serves as a hermitically sealed surface prior to the deposition of the subsequent film. This densified film layer is not uniform, with respect to film thickness and composition, across the wafer and also within the thickness of the altered surface. This creates an extremely rough interface for the subsequent reactive-ion-etch (RIE) patterning. This results in micromasking during the RIE processing and results in an undesirable final structure. Micromasked structures can lead to premature device reliability fails. The presence of the densified layers within the hardmask or the hardmask-pOSG film interface can be addressed by using aggressive RIE process conditions. However, this is detrimental towards the pOSG films that cannot withstand aggressive RIE conditions.

It would therefore be desirable to provide an interconnect structure, that can provide robust adhesion at the interface of the hardmask and pOSG film without changing the bulk of the pOSG film. This allows for the integration of pOSG in an interconnect structure. It would also be desirable for the hardmask stack to possess no intermediate densified layers that could lead to

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micromasked structure in the final interconnect structure. The absence of densified layers, within the hardmasks and at the hardmask-pOSG film interface, enhances the RIE process window and allows for gentler RIE conditions.

5

SUMMARY

10 It is therefore an object of the present invention to provide a film structure, comprising of a pOSG film, that would enable the fabrication of a BEOL interconnect structure of, e.g., the single Damascene and dual Damascene type, in both the thinwire and fatwire levels.

It is also an object of the present invention to provide a BEOL interconnect structure with robust adhesion between the pOSG surface and the hardmask.

15 It is also an object of the present invention to provide a BEOL interconnect structure with improved adhesion between the hardmask films while eliminating buried densified layers. These densified layers often results in severe micromasking effects during the RIE patterning of the interconnect structure.

In keeping with these objects of the present invention, there is provided a method for 20 fabrication of an unique structure using pOSG and appropriate hardmasks. This is accomplished by:

a. ensuring robust adhesion of the hardmask material to the pOSG;

b. using plasma treatments to change the surface morphology of the pOSG films to enhance the adhesion between the hardmask and the pOSG film;

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c. ensuring pOSG film does not become damaged during the plasma treatments;

d. tailoring the interfaces between the sacrificial interfaces such that micromasking is eliminated during the RIE processes.

A method for making an interconnect structure with pOSG having substantially enhanced adhesion and minimal micromasking has also been discovered which comprises the following sequence of steps:

a. surface modification of the morphology of the pOSG film through non-damaging plasma treatments, the main role of which is to chemically activate the surface of the pOSG film;

b. deposit, in-situ or ex-situ, an appropriate hardmask, such as SiC, SiCH, SiCN, SiCOH, that serves as a hermetically sealed dielectric film;

c. deposit, in-situ or ex-situ, another dielectric hardmask stack, unitary or hybrid, in order to protect the first hardmask and the patterning photoresist from each other, without changing the surface of the first hardmask dielectric film,

d. eliminate all buried densified layers in the hardmask stack.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention are believed to be novel, and the elements characteristics of the invention are set forth in the appended claims. The figures are for illustration purposes and are not drawn to scale. The preferred embodiments of the present disclosure are described below with reference to the drawings, which are described as follows:

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FIG. 1 is a schematic cross-sectional view of the interconnect structure with a densified layer within the hardmask stack;

FIG. 2 is a schematic cross-sectional view of the interconnect structure of FIG. 1 showing the effect of micromasking, during the RIE patterning of the dielectric structure;

FIG. 3 is a schematic cross-sectional view of an alternative embodiment of the interconnect structure of FIG. 1, showing the desired smooth etch front required in the patterning of the interconnect structure.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention is directed to an interconnect structure useful for forming a semiconductor device, the interconnect structure having a low-k pOSG dielectric layer, and depositing the associated low-k hardmask dielectric stack. Enhanced adhesion between the pOSG dielectric film and the hardmask dielectric stack is achieved by means of a mild plasma surface treatment of the pOSG film surface. Typically, it has been observed and reported widely in literature that plasma treatment of pOSG films lead to an overall increase of the dielectric constant indicating damage of the pOSG material. This damaged layer causes an increase in the capacitance and leakage within the dielectric material, when subjected to an electric stress, which leads to reliability failure of the interconnect structure.

The interconnect structure of the present invention is based on the surprising discovery that particular plasma conditions, used to enhance the adhesion of the dielectric material to the hardmask dielectric material, did not cause an increase in the dielectric constant of the pOSG film or result in leakage in the structure. Additionally, it was also discovered that removing all

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the densified layers within the hardmask stack resulted in micromasking-free structures, while maintaining the integrity of the hardmask dielectric stack. The interconnect structure of the present invention will now be described in more detail by referring to the drawings accompanying the present application.

Referring now to FIG. 1, one such semiconductor device in accordance with the present disclosure can be formed by first providing an integrated circuit structure 1 which is formed in a semiconductor material substrate. The expression "integrated circuit structure" as used herein refers to, for example, an integrated circuit at the end of its formation as is known in the art, i.e., after formation of metallization strips. The substrate may be a semiconductor wafer or chip which is composed of any silicon-containing semiconductor material such as, for example, Si, SiGe, Si/SiGe, $Si/SiO_2/Si$, etc. The substrate may be of the n or p-type depending on the desired device to be fabricated. Moreover, the substrate may contain various isolation and/or device regions either formed in the substrate or on a surface thereof. The substrate may also contain metallic pads on the surface thereof. In addition to silicon-containing semiconductor materials, the substrate may also be a circuit that includes CMOS devices therein.

Referring again to FIG. 1, a dielectric material 2, herewith referred to as the cap layer, is deposited on top of the integrated circuit 1 in order to serve as a protection layer by encapsulating the underlying integrated circuit 1. The main role of this cap layer is to protect the underlying material from oxidants, moisture, and ionic contamination. Depending on the nature of the material and its effectiveness in performing as a diffusion barrier, the thickness of this material 2 can vary from a couple of nanometers to few-tens of nanometers. This layer can be made of any suitable capping material, such as silicon nitride, silicon carbide, silicon oxycarbide, hydrogenated silicon carbide, silicon dioxide, organosilicate glass, and other low-k dielectric materials. This layer 2 can also be used as an etch stop during the patterning of ILD 3.

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Any organosilicate (OSG) material can be used as ILD 3, herewith referred to as ILD or OSG or pOSG. In particular, a material with dielectric constant values of less than 3 is preferred. As commonly known by those skilled in the art, typical materials that fall is the class of k<3 tend to be porous. The average pore size and size distribution of these materials will ordinarily range from about 1 to about 25 nm, with less than about 5 nm being preferred.

As commonly known by those skilled in the art, one of the major problems with the integration of the OSG materials as ILD, is the poor adhesion with the hardmask dielectric material 5, herewith referred to as lower hardmask. This hardmask material serves multiple purposes, as known to those skilled in the art, such as chemical-mechanical polish (CMP) stopping layer, a barrier to protect the porous-OSG (pOSG) material from moisture and slurry solvents, and a template to enable the patterning of the pOSG material. This layer can be made of any suitable material, such as silicon nitride, silicon carbide, silicon oxycarbide, hydrogenated silicon carbide, silicon dioxide, organosilicate glass, and other low-k dielectric materials.

One commonly known method, which has been historically being used, to improve the adhesion between two smooth interfaces is to roughen the interfaces. This roughening increases the surface area available to promote the adhesion of these two surfaces. The second method, to improve adhesion, is to chemically modify the surface of one of the films by creating reactable dangling bonds that is used to chemically link or bond to the second film. One method of achieving these objectives in thin-film technology is to plasma-treat the ILD film surface.

pOSG materials, due to the high degree of porosity, offers a rough surface at the nanometer scale. The adhesion to the hardmask material, in spite of the ILD's rough texture and high surface area, is poor. So the necessity of a plasma treatment becomes necessary to create the reactable dangling bonds on the surface of the pOSG film (3) in order to promote the bonding of the hardmask material 5. This is shown as a separate layer in FIG. 1 as layer 4, herewith

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referred to as plasma altered pOSG layer. A requirement of the plasma treatment is that pOSG dielectric (3) should not be damaged. This limits the choice of appropriate plasma conditions in terms of the plasma gas, operating power and the duration of exposure. SEMATECH has shown that the exposure of the pOSG dielectric (3) for 0.5s six-times at a plasma power of 1000W is sufficient to enable the adhesion of the hardmask material. However, there are two drawbacks in this approach, i.e., the instability of plasma conditions in 0.5s duration and the damage to the pOSG film due to the high power density. The altered pOSG layer 4, under the SEMATECH condition, raises the effective dielectric constant of the pOSG film and negates the introduction of a lower-k dielectric material.

Investigation of the plasma conditions was undertaken, where the choice of gas was limited to light gases such as, hydrogen (H_2), helium (He) and nitrogen (N_2), the plasma power was varied from 100W to 250W and the duration was varied from 1s to 30s. More damage was caused, in terms of dielectric constant of the pOSG film, when heavier gases such as nitrogen were used or when the duration of plasma exposure was too long. The net increase in the dielectric constant of the pOSG with the altered layer was greater than 10%. This was expected due to the damaging nature of the plasma conditions.

The surprising finding of the study, that forms the core of this disclosure, is the existence of a process window for the plasma conditions which resulted in greater than 15% improvement in the adhesion of the hardmask without any measurable change in the dielectric constant. The conditions included the use of H_2 or He as the gas, limiting the plasma power to less than 200W and plasma exposure to less than 10s. These conditions prove to be very useful in modifying the morphology of the surface of the pOSG film (3) to enable adhesion to the lower hardmask without changing the bulk of the pOSG material (3). Additionally, it was also observed that keeping the interface clean after the plasma treatment lent itself to better adhesion conditions to

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the lower hardmask, and hence this imposed that the lower hardmask be deposited in-situ after the plasma-altering of the pOSG surface.

Keeping in view of the fact that hardmask 5 is retained after CMP, it is advantageous to have a low-k material as the hardmask, so as to keep the effective dielectric constant of the entire stack low. The major drawback of this requirement is that the materials that satisfy this condition are susceptible to photoresist rework conditions that typically involve oxygen-based plasma strip conditions. Hence, in order to protect this hardmask layer 5 from damaging photoresist strip conditions, another protective hardmask dielectric layer 6, herewith referred to as upper hardmask, is deposited on top layer 5. This material, depending on the integration scheme, could be a single material or a hybrid material. This layer can be made of any suitable material that withstands photoresist rework conditions, such as silicon nitride, silicon dioxide, silicon oxy-nitride, tantalum nitride, and titanium nitride. As can be appreciated by those skilled in the art, these materials are either high-k or metallic, and hence should be completely sacrificial, i.e., should be completely removed after CMP in order to preserve the integrity of the structure.

Typically, an ex-situ deposition of the upper hardmask, involves the use of a reactive plasma clean step prior to the deposition of the hardmask material that would damage the bulk of the low-k lower hardmask material 5. In order to prevent this damage, the surface of the lower hardmask 5 is often densified in inert-gas plasma, such as He plasma. This is shown in FIG. 1 as a separate layer 7, herewith referred to as the plasma densified layer. Analogous to the pOSG plasma altered layer 4, layer 7 may also be used to promote adhesion within the hardmask layers. As stated earlier, the advantage of this densified layer 7 is that it readily encourages ex-situ deposition of the upper hardmask 6.

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FIG. 1 shows a structure that has at least two modified layers, i.e., layers 4 and 7. One of the major issue in the fabricating these structures is that these layers may adversely influencing the patterning process. These layers are spatially non-uniform in composition and morphology and pose a serious challenge in reactive ion etch (RIE) patterning of the pOSG structure as shown in FIG. 2 as 8. As can be appreciated by those skilled in the art, a gradation in the composition of a material could significantly change the etch rate of the material during RIE. So a non-uniform lateral and spatial composition of the densified films locally alters the etch rate of the material. This non-uniformity results in a micromasked profile as shown in FIG. 2 as 9, herewith referred to as micromasks.

An embodiment of this invention relates to maintaining the requirements posed by deposition of hardmask films, while trying to attain smooth etch front without the occurrence of micromasks. In the case of the deposition of the hardmasks, it was found that eliminating the plasma densified layer 7 (FIG. 2) leads to a dramatic reduction of micromasks. This, however, poses a problem, wherein deposition of the upper level hardmasks could not be achieved without damaging the lower surface through plasma clean of the lower hardmask. This problem was immediately alleviated by depositing the upper level hardmask in-situ on the lower level hardmask. The surprising find of this study resulted in the find that the hardmask survived CMP processes up to a pad down-force of 5 psi., whereas, it was expected that the adhesion would be very weak. Taking the film stack through RIE, by eliminating layer 7, resulted in smooth etch fronts in pOSG. This result is shown in layer 10 in FIG. 3.

Another embodiment of this invention involves the plasma altered layer 4, which did not influence the etch front in pOSG (3). This suggests, that the plasma conditions used in improving the adhesion of the lower hardmask (5) to the pOSG film (3), did not alter the

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morphology and microstructure beyond the surface of the pOSG surface (4), to an extent where it caused micromasking effects, while still modifying the surface to improve adhesion.

Hence, this invention includes a method of building a structure, encompassing a pOSG material, wherein, the surface of pOSG was altered to increase adhesion to the hardmask material without affecting the RIE patterning process, and a method of depositing the relevant hardmasks, in-situ, without forming intermediate densified layers that cause micromasked profiles. Although the invention has been described in its preferred form with a certain degree of particularity, obviously many changes and variations are possible therein and will be apparent to those skilled in the art after reading the foregoing description. For example, additional layers known in the art can be formed on the top of hardmask 6. It is therefore to be understood that the present invention may be presented otherwise than as specifically described herein without departing from the spirit and scope thereof.

WHAT IS CLAIMED IS:

1. An interconnect structure comprising:
   a. one or more interconnect levels, one on top of each other, with each level comprising of a OSG low-k dielectric material.
   b. one or more interconnect levels, one on top of each other, with each level comprising of a OSG low-k dielectric material and an inorganic material as the hardmask material.

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c. one or more interconnect levels, one on top of each other, with each level comprising of a OSG low-k dielectric material and an inorganic material as the capping material.

2. An interconnect structure of Claim 1 comprising of the fabrication of an interconnect layer.

3. The interconnect structure of Claim 1 wherein the OSG layer comprises a non-porous or porous material having a dielectric constant less than 3.

4. The interconnect structure of Claim 3 wherein the OSG layer could compose of a combination of porous and non-porous OSG materials.

5. The interconnect structure of Claim 3 wherein the OSG layer comprises of a material of Si, C, O and H and having a dielectric constant less than about 3.

6. The interconnect structure of Claim 3 wherein the atomic composition of the OSG material is about 10 to about 40% Si, about 10 to about 40% C, about 15 to about 45% O, and about 20 to about 50% H.

7. The interconnect structure of Claim 3 wherein the porosity of the OSG layer is about 0% to about 70%.

8. The interconnect structure of Claim 3 wherein the pore size of the OSG layer is about 0.2nm to about 20nm.

9. The interconnect structure of Claim 1 wherein the cap layer comprises of a material of Si, C, N and H and having a dielectric constant less than about 5.

10. The interconnect structure of Claim 9 wherein the material comprising Si, C, N and H possesses an atomic composition of about 10 to about 40% Si, about 0 to about 30% C, about 0 to about 30% N, and about 20 to about 50% H.

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11. The interconnect structure of Claim 1 wherein the cap layer encapsulates the finished metallized layer which comprises of the OSG low-k material.

12. The interconnect structure of Claim 11 wherein the cap layer is a diffusion barrier that prevents the interaction of Cu with the next layer dielectric material.

13. The interconnect structure of Claim 11 wherein the cap layer is a diffusion barrier that prevents the interaction of oxidants with the metallized layer.

14. The interconnect structure of Claim 11 wherein the cap layer is a diffusion barrier that prevents the interaction of oxidants with the lower level patterned dielectric layer.

15. The interconnect structure of Claim 1 wherein the next layer low-k OSG material is deposited on the cap layer to form the next-layer structure.

16. The interconnect structure of Claim 15 wherein the deposition of the OSG material occurs in-situ on the cap layer.

17. The interconnect structure of Claim 15 wherein the deposition of the OSG material occurs ex-situ on the cap layer.

18. The interconnect structure of Claim 15 wherein the characteristics of the OSG material is described in Claim 5, Claim 6, Claim 7 and Claim 8.

19. The interconnect structure of Claim 1 wherein the lower hardmask layer comprises of a material of Si, C, O and H and having a dielectric constant less than about 5.

20. The interconnect structure of Claim 1 wherein the lower hardmask layer comprises of a material of Si, C, O, H and N and having a dielectric constant less than about 5.

21. The interconnect structure of Claim 19 wherein the atomic composition of the inorganic dielectric material is about 10 to about 40% Si, about 10 to about 40% C, about 0 to about 45% O, and about 25 to about 55% H.

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22. The interconnect structure of Claim 20 wherein the atomic composition of the inorganic dielectric material is about 10 to about 40% Si, about 10 to about 40% C, about 0 to about 45% O, about 25 to about 55% H and about 5 to about 25% N.

23. The interconnect structure of Claim 1 wherein the lower hardmask layer is deposited on the OSG low-k material.

24. The interconnect structure of Claim 23 wherein the lower hardmask layer encapsulates the OSG low-k material.

25. The interconnect structure of Claim 23 wherein the lower hardmask layer is a stopping layer for chemical-mechanical polish.

26. The interconnect structure of Claim 23 wherein the deposition of the hardmask material occurs in-situ on the OSG layer.

27. The interconnect structure of Claim 23 wherein the deposition of the hardmask material occurs ex-situ on the OSG layer.

28. The interconnect structure of Claim 23 wherein the deposition of the hardmask material is preceded by a plasma treatment of the OSG surface.

29. The interconnect structure of Claim 28 wherein plasma treatment of the OSG surface is used to enhance the adhesion of the lower hardmask to the OSG surface.

30. The interconnect structure of Claim 29 wherein the adhesion improved by greater than 10% with the use of the plasma treatment.

31. The interconnect structure of Claim 28 wherein the deposition of the hardmask material occurs in-situ after a plasma treatment of the OSG surface.

32. The interconnect structure of Claim 28 wherein the deposition of the hardmask material occurs ex-situ after a plasma treatment of the OSG surface.

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33. The interconnect structure of Claim 28 wherein the plasma treatment does not chemically change the bulk of OSG film.

34. The interconnect structure of Claim 28 wherein the plasma treatment does not alter the electrical characteristics of the OSG film.

35. The interconnect structure of Claim 34 wherein the change in the dielectric constant of the OSG film is less than 0.05.

36. The interconnect structure of Claim 28 obtained through Claim 29, Claim 30, Claim 33 Claim 34 and 35.

37. The method of Claim 34 obtained by using plasma conditions wherein the feed gas is a low atomic-mass element.

38. The method of Claim 37 obtained by using plasma conditions wherein the feed gas is H_2 (Hydrogen).

39. The method of Claim 37 obtained by using plasma conditions wherein the feed gas is He (Helium).

40. The method of Claim 36 obtained by using plasma conditions wherein the operating pressure is about 0.1 Torr to about 10 Torr.

41. The method of Claim 36 obtained by using plasma conditions wherein the plasma power is below 200Watt.

42. The method of Claim 36 obtained by using plasma conditions wherein the duration of plasma is below 10 seconds.

43. The interconnect structure of Claim 36 wherein the plasma treatment of the OSG surface does not induce micromasking during reactive ion etch patterning of the structure.

44. The interconnect structure of Claim 15 obtained through the fabrication steps involving:

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a. deposition of OSG layer on the cap layer,

b. plasma-treatment of the OSG surface to improve adhesion to next layer,

c. deposition of the bottom hardmask on the plasma-treated OSG surface.

45. The interconnect structure of Claim 44 wherein the deposition steps involved could all be in-situ.

46. The interconnect structure of Claim 44 wherein the deposition steps involved could all be ex-situ.

47. The interconnect structure of Claim 44 wherein the deposition of the various layers involved could be a combination of in-situ and ex-situ steps.

48. The interconnect structure of Claim 1 and Claim 44 wherein the fabrication structure involved to form the interconnect structure involves the deposition of upper hardmask material.

49. The interconnect structure of Claim 48 wherein the upper hardmask is formed of one or more material layers.

50. The interconnect structure of Claim 48 wherein the upper hardmask is resistant to photoresist rework.

51. The interconnect structure of Claim 48 wherein the upper hardmask layer is formed from a material selected from the group consisting of Si_3N_4, $Si_xO_yN_z$, SiO_2, Ta_xN_y or Ti_xN_y.

52. The interconnect structure of Claim 48 wherein the upper hardmask can be completely sacrificial, i.e., is completely removed during chemical-mechanical polishing.

53. The interconnect structure of Claim 48 wherein the upper hardmask is deposited in-situ on the lower hardmask.

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54. The interconnect structure of Claim 48 and Claim 53 wherein the removal of plasma densification of the lower hardmask surface does not cause adhesion failure with the upper level hardmask layer.

55. The interconnect structure of Claim 44 wherein a unique fabrication structure involving the steps of:

a. deposition of OSG layer on the cap layer,

b. plasma-treatment of the OSG surface to improve adhesion to next layer,

c. deposition of the bottom hardmask on the plasma-treated OSG surface,

d. deposition of the upper hardmask on non-plasma treated lower hardmask surface.

56. The interconnect structure of Claim 55 and other aforementioned claims wherein the adhesion of the various layers comprising the interconnect stack is enhanced than without implementing the claims presented.

57. The interconnect structure of Claim 55 and other aforementioned claims wherein the altered interfaces obtained through the claims presented in this invention does not cause micromasks during the patterning of the dielectric stack.

58. The method of fabricating an interconnect structure of Claim 55, Claim 57 and other aforementioned claims wherein gentle RIE chemistries can be implemented in order to form a pattern in the film stack.

59. The method of Claim 58 wherein gentle RIE chemistries reduce damage to the OSG material.

60. The interconnect structure of Claim 55 and other aforementioned claims wherein fabrication of a metallized structure is achieved without electrically damaging or altering the OSG film layer.

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ABSTRACT

Novel interconnect structure having enhanced adhesion between the various interfaces, encompassing a porous organo-silicate glass (pOSG) film, for use in semiconductor devices in provided herein. The novel interconnect structure comprises of a non-damaging plasma-treatment of the low-k pOSG surface to enhance the adhesion of the hardmask material to the pOSG surface, and an unique deposition scheme for the hardmasks in order to make the entire structure pliant towards implementing mild processing condition during the reactive ion etch patterning of the dielectric structure in a Damascene and dual-Damascene scheme. The methods for making a semiconductor device having an enhanced adhesion and micromasks free profiles are also provided.

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FIG. 1

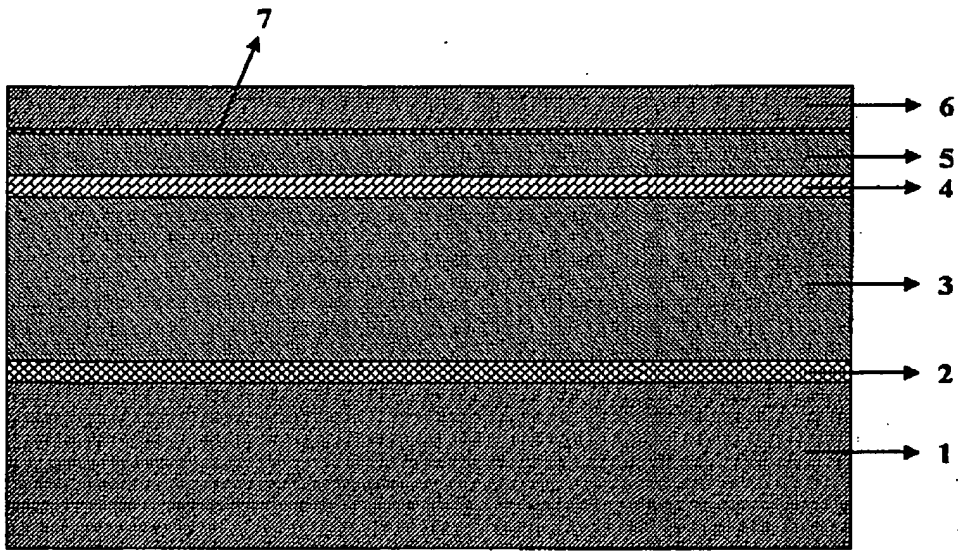

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FIG. 2

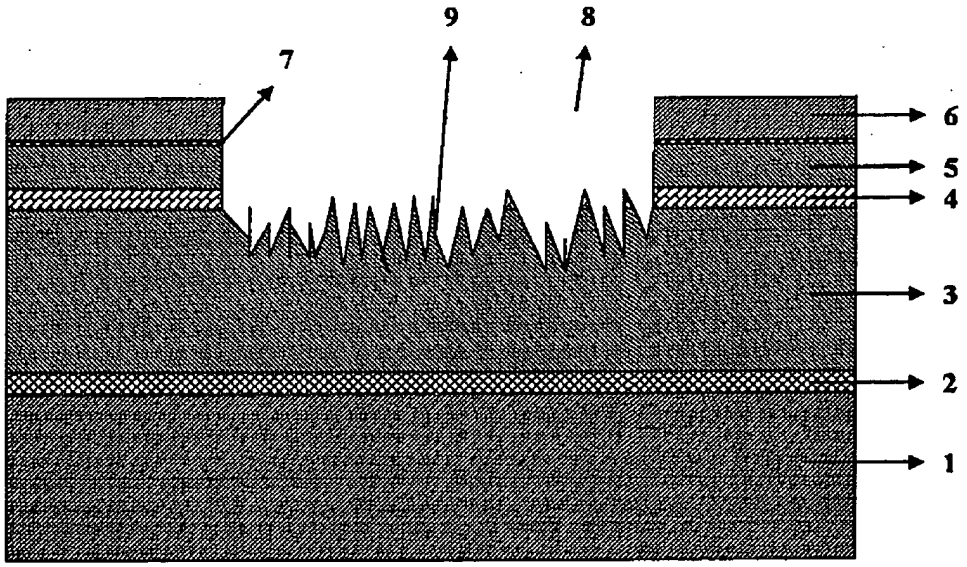

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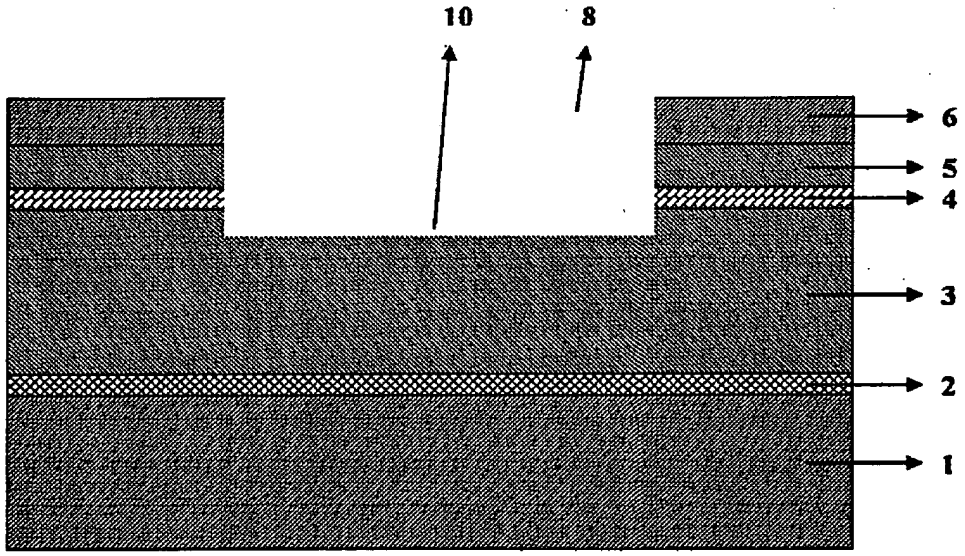
FIG. 3



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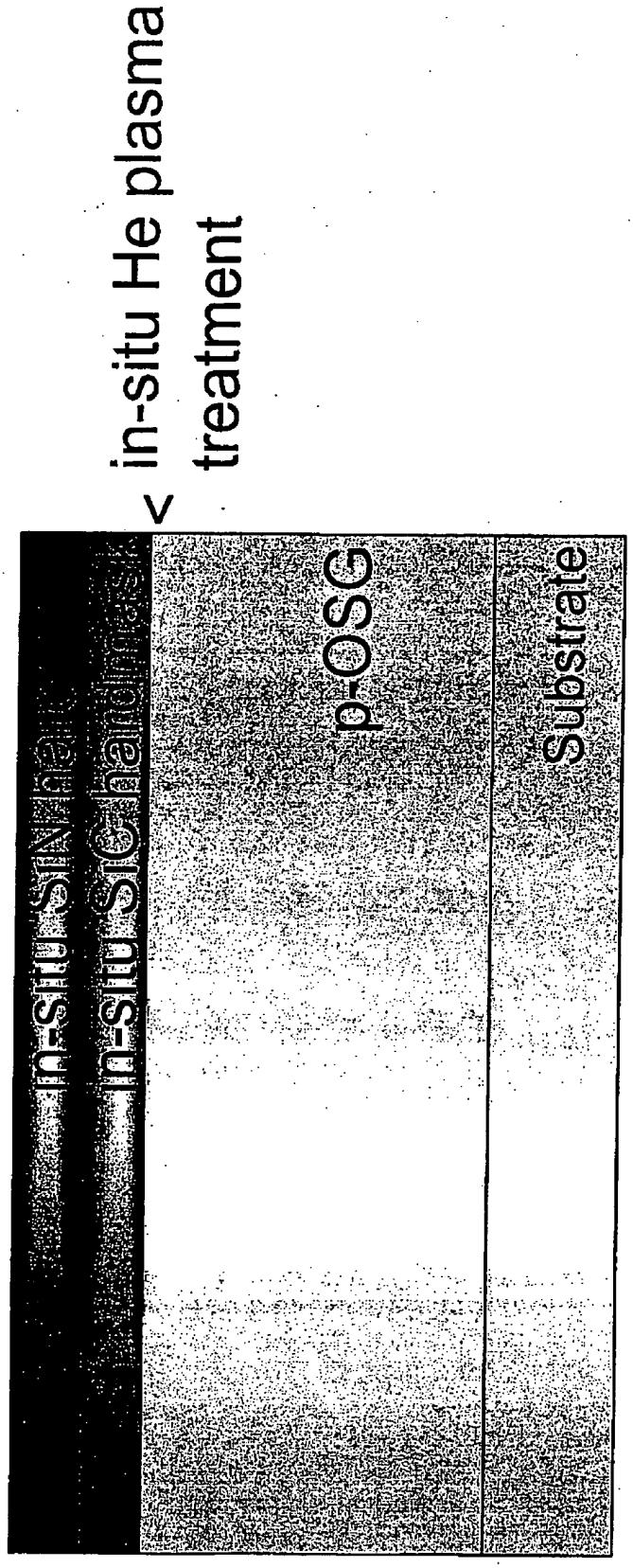
Novel RIE hardmask processing to eliminate RIE micromasking while maintaining hardmask adhesion



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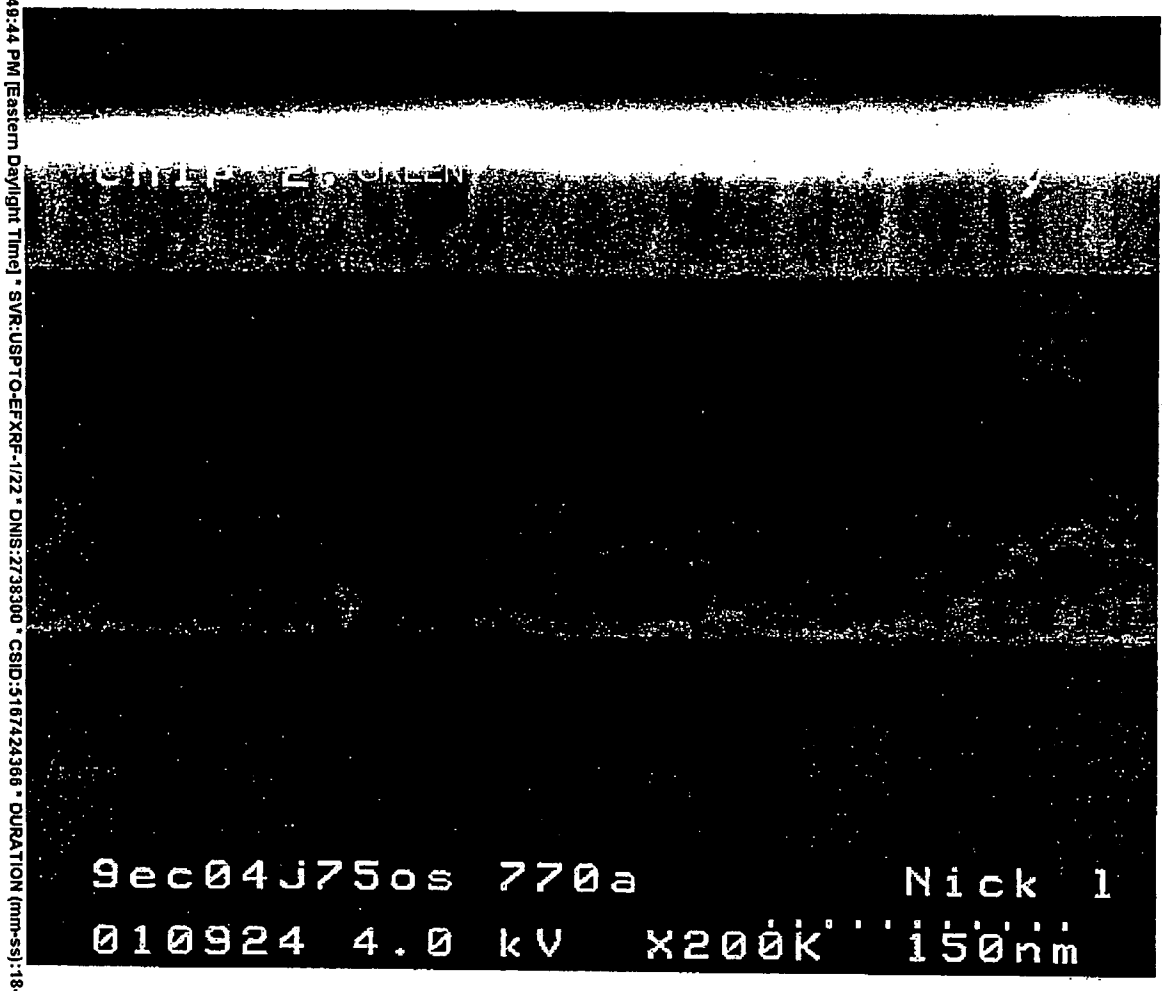
Actual ASTC Build

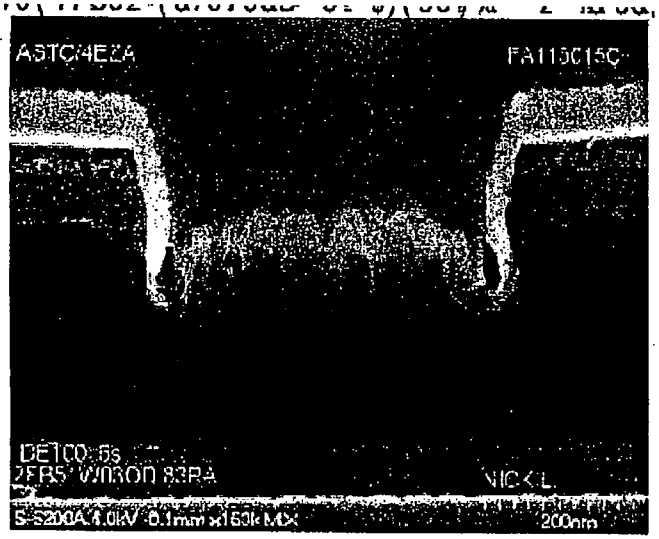


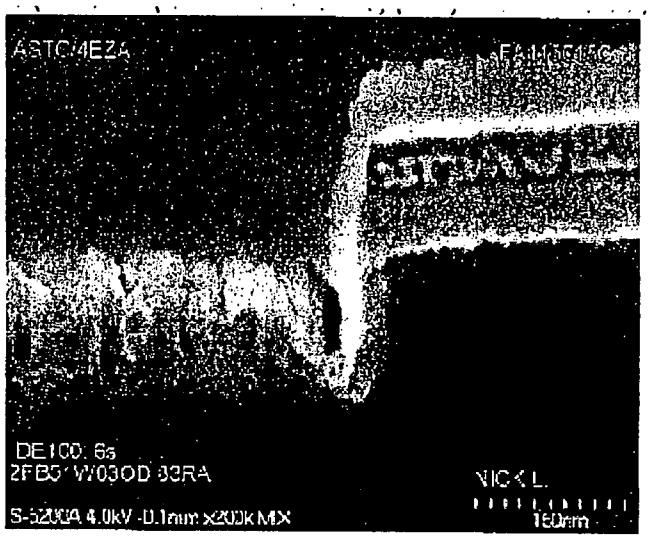
< Au from SEM prep

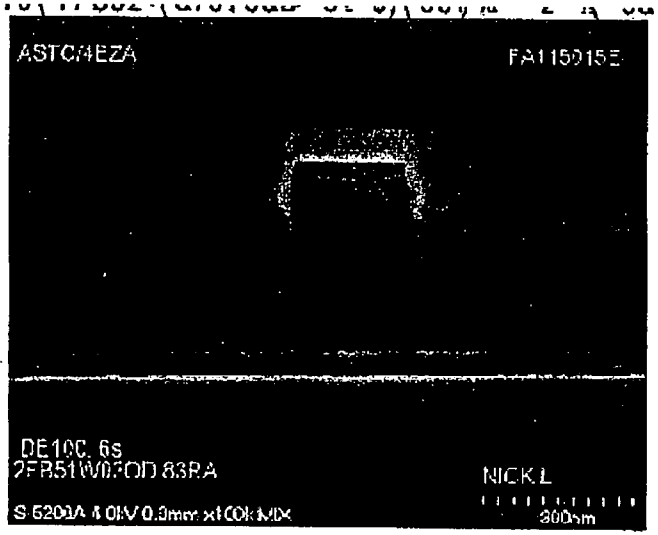
< p-OSG modification due to He treatment, enhanced adhesion

< p-OSG

RIE micromasking after SiC open with densified SiC and ex-situ SiN







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No RIE micromasking after SiC open with non-densified SiC and in-situ SiN